This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A reconfigurable emulation integrated circuit, comprising:

a storage unit comprising a signal inclusion schedule; and

circuitry, coupled to the storage unit, operative to generate and transmit a message outside the reconfigurable emulation integrated circuit, the message assembled in accordance with the signal inclusion schedule and comprising a plurality of emulation signals, wherein the signal inclusion schedule selects the plurality of emulation signals from at least one pin when the message is assembled and specifies the order and frequency of occurrence of each of the plurality of emulation signals in the message.

Claim 2 (Currently Amended): The reconfigurable emulation integrated circuit of claim 1, wherein the frequency of occurrence specified by the signal inclusion schedule is based on a determination that particular emulation signals in ~~a~~ the message ~~that are determined to be~~ are more critical than other emulation signals in the message, and the particular emulation signals that are more critical occur in the message with greater frequency ~~than signals~~ than the other emulation signals in the message ~~determined to be less critical in the signal inclusion schedule~~.

Claim 3 (previously presented): The reconfigurable emulation integrated circuit of claim 1, wherein the message is generated and transmitted in a plurality of clock cycles of an operating clock that is independent of an emulation clock of the plurality of signals.

Claim 4 (previously presented): The reconfigurable emulation integrated circuit of claim 1, wherein the circuitry further includes a parity value generator and wherein the message further comprises a parity value generated by the parity value generator.

Claims 5-8 (canceled)

Claim 9 (Currently Amended): A reconfigurable integrated circuit, comprising:

a storage unit comprising a signal inclusion schedule for a plurality of emulation signals to be received in a message, the plurality of emulation signals selected from at least one pin when the message is assembled; and

circuitry, coupled to the storage unit, operative to receive the message and extract the plurality of emulation signals from the message in accordance with the signal inclusion schedule, wherein the signal inclusion schedule specifies the order and frequency of occurrence of each of the plurality of emulation signals in the message.

Claim 10 (Currently Amended): The reconfigurable emulation integrated circuit of claim 9, wherein the frequency of occurrence specified by the signal inclusion schedule is based on a determination that particular emulation signals in ~~a~~ the message ~~that~~ are ~~determined to be~~ more critical than other emulation signals in the message, and the particular emulation signals that are more critical occur in the message with greater frequency than the other emulation signals in the message ~~determined to be less critical in the signal inclusion schedule~~.

Claim 11 (Currently Amended): The reconfigurable emulation integrated circuit of claim 9, wherein the message comprises state values of the plurality of emulation signals.

Claim 12 (Currently Amended): The reconfigurable emulation integrated circuit of claim 9, wherein the message is received and disassembled in a plurality of clock cycles of an operating clock that is independent of an emulation clock of the plurality of emulation signals.

Claim 13 (previously presented): The reconfigurable emulation integrated circuit of claim 9, wherein a parity value is extracted from the message.

Claim 14 (Currently Amended): The reconfigurable emulation integrated circuit of claim 13, wherein the circuitry is further configured to generate a parity verification value from the extracted plurality of emulation signals and compare the parity verification value with the extracted parity value.

Claims 15-19 (canceled)

Claim 20 (Currently Amended): An emulation integrated circuit, comprising:

at least one reconfigurable logic resource;

at least one output pin; and

a message formation and send block in communication with the output pin and the reconfigurable logic resource, the message formation and send block operative to receive ~~multiple output~~emulation signals from the reconfigurable logic resource and generate a message on the output pin in accordance with a first signal inclusion schedule that selects at least one of the ~~multiple output~~emulation signals when the message is generated, wherein the first signal inclusion schedule specifies the order and frequency of occurrence of each of the ~~output~~ emulation signals in the message.

Claim 21 (Currently Amended): The emulation integrated circuit of claim 20, further comprising:

an input pin; and

a message receive and disassembly block in communication with the input pin and the reconfigurable logic resource, operative to receive a message and extract ~~multiple input~~second emulation signals from the message in accordance with a second signal inclusion schedule.

Claim 22 (Currently Amended): The emulation integrated circuit of claim 20, further comprising a ~~plurality~~ second ~~of~~ output ~~pins~~ pin and a ~~plurality~~ second ~~of~~ message formation and send block~~s~~ in communication with the ~~plurality of output pins~~second output pin and the reconfigurable logic resource, ~~each~~ the second message formation and send block operative to receive ~~multiple output~~emulation signals from the reconfigurable logic resource and generate a second message on the output pin in accordance with a different ~~respective~~ signal inclusion schedule.

Claim 23 (original): The emulation integrated circuit of claim 20, further comprising a plurality of reconfigurable logic resources in communication with the message formation and send block.

Claim 24 (Currently Amended): An emulation integrated circuit, comprising:

at least one reconfigurable logic resource;

at least one input pin; and

a message receive and disassembly block in communication with the reconfigurable logic resource and the input pin, the message receive and disassembly block operative to receive a message assembled from a selection of ~~multiple input~~emulation signals from at least one pin when the message is assembled in accordance with a first signal inclusion schedule, wherein the message is received at the at least one input pin and the ~~multiple input~~emulation signals are extracted for the at least one reconfigurable logic resource in accordance with a second signal inclusion schedule, wherein the second signal inclusion schedule specifies the order and frequency of occurrence of each of the ~~input~~ emulation signals in the message.

Claims 25-27 (canceled)

Claim 28 (previously presented): The emulation integrated circuit of claim 24, wherein the first signal inclusion schedule and the second signal inclusion schedule are different signal inclusion schedules.

Claim 29 (previously presented): The emulation circuit of claim 24, wherein the first signal inclusion schedule comprises a message send schedule and the second signal inclusion schedule comprises a message receive schedule.

Claim 30 (previously presented): The reconfigurable emulation integrated circuit of claim 1, wherein the message is generated and transmitted for a number of clock cycles of an operating clock, and the signal inclusion schedule is determined to provide a number of signal selections equal to the number of clock cycles.

Claim 31 (previously presented): The reconfigurable emulation integrated circuit of claim 1, wherein the message is generated and transmitted for a number of clock cycles of an operating clock, and the signal inclusion schedule is determined to provide a number of signal selections less than the number of clock cycles.

Claim 32 (previously presented): The reconfigurable emulation integrated circuit of claim 2, wherein the order specified by the signal inclusion schedule is determined based on the determined frequency of occurrence.